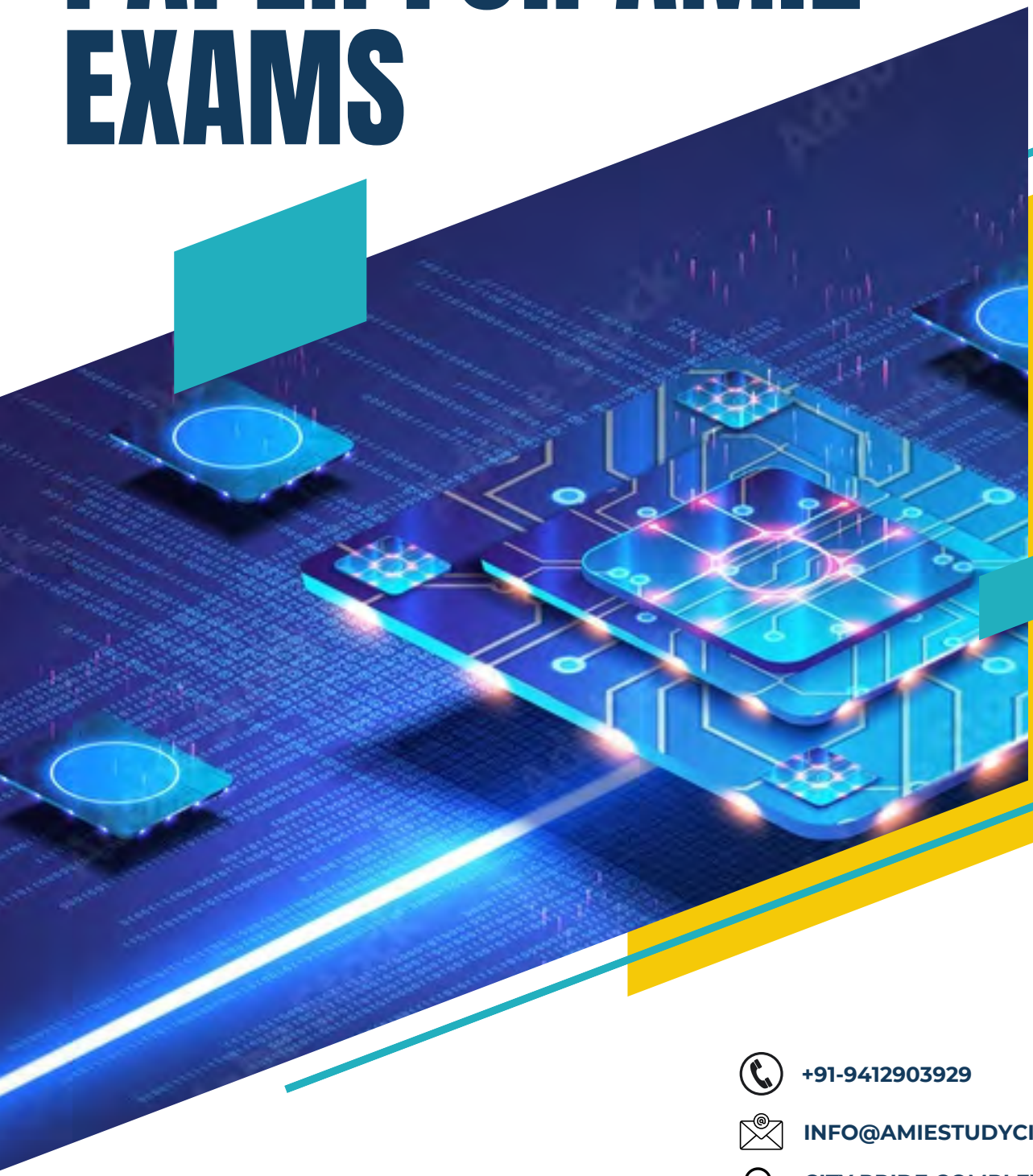
AMIE STUDY CIRCLE, ROORKEE

MODEL TEST PAPER FOR AMIE EXAMS



COMPUTER ARCHITECTURE

TEST PAPER 1

+91-9412903929

INFO@AMIESTUDYCIRCLE.COM

CITY PRIDE COMPLEX, NR IIT CAMPUS, ROORKEE

AMIESTUDYCIRCLE.COM

COMPUTER ARCHITECTURE

***Time**: Three Hours*

***Maximum Marks**: 100*

Answer five questions, taking ANY TWO from Group A, any two from Group B and all from Group C.

All parts of a question (a, b, etc.) should be answered at one place.

Answer should be brief and to-the-point and be supplemented with neat sketches.

Unnecessary long answer may result in loss of marks.

Any missing or wrong data may be assumed suitably giving proper justification.

Figures on the right-hand side margin indicate full marks.

Group A

1. (a) Write a short note on the stack organisation. How can it be implanted? Give example. 6

   (b) What is the difference between zero-address, one-address and two-address instructions ? Illustrate with the help of examples. 6

   (c) Discuss two different types of addressing modes with examples of their usage. 8

2. (a) What is the role of a control unit in a processor? What is the difference between a hardwired control unit and a microprogrammed control unit? Explain the relative advantages of a hardwired and a microprogrammed control unit. 10

   (b) What is meant by a hardwared implementation of a control unit? Explain briefly. 10

3. (a) Explain the concept of a memory hierarchy. What is the advantage of hierarchical memory system? 6

   (b) What do you understand by Memory Management Unit (MMU)? What is its role? 6

   (c) Explain the working of associative memory with a neat diagram. 8

4. (a) Explain the operation of DMA using a block diagram. Discuss DMA transfer with a suitable block diagram. 10

   (b) Differentiate between synchronous and asynchronous bus (communication). What are their relative advantages? 10

Group B

5. (a) What is pipelining? Distinguish between a instruction pipeline and an arithmetic pipeline? Determine the speed up that can be achieved by a 5-stage instruction pipeline in executing 100 instructions over a comparable non-pipeline processor. 10

   (b) What are different pipeline hazards? Explain each pipeline hazard. 10

6. (a) What is a vector pipeline? Explain the organization of a vector pipeline using a neat block diagram. 10

   (b) A non-pipeline system lakes 60 ns to process a task. The same task can be processed in six-segment pipeline with a clock cycle of 10 ns. Determine the speed up ratio of pipeline for 100 tasks What is the maximum speed up that can be achieved? 10

7. (a) Discuss Flynn's classification of computer architectures with diagrams. 10

   (b) What are multiprocessors? Explain using a block diagram. 10

8. (a) Using a suitable block diagram, explain the architecture of a SIMD computer. Identify at least two applications for which SIMD computers are suitable. 8

   (b) Explain loosely coupled and tightly coupled microprocessors, and discuss their relative advantages. 6

   (c) Why is hypercube interconnection network popular? Compare it with omega and shuttle exchange interconnection networks. 6

Group C

9. Answer the following in brief: 20

(i) Define miss penalty.

(ii) What is a circular buffer?

(iii) Differentiate between processor and coprocessor.

(iv) What is Bit-O Ring technique?

(v) Differentiate between maskable and non-maskable interrupts.

(vi) Mention one advantage of memory interleaving.

(vii) Cache hit ratio

(viii) Data flow computer

(ix) What do you mean by the term 'speed up'? Explain your answer using an example.

(x) What is the reason for cache memory to be faster than main memory?

(Refer our course material for answers)